

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
21 July 2005 (21.07.2005)

PCT

(10) International Publication Number
WO 2005/066969 A1

(51) International Patent Classification⁷: **G11C 11/56**,
11/34, H01L 45/00

(74) Agents: **MAEDA, Hiroshi** et al.; Osaka-Marubeni Bldg.,
5-7, Hommachi 2-chome, Chuo-ku, Osaka-shi, Osaka
5410053 (JP).

(21) International Application Number:
PCT/JP2004/016082

(22) International Filing Date: 22 October 2004 (22.10.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2003-435269 26 December 2003 (26.12.2003) JP
2004-131542 27 April 2004 (27.04.2004) JP
2004-167223 4 June 2004 (04.06.2004) JP

(71) Applicant (for all designated States except US): **MAT-
SUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
[JP/JP]; 1006, Oaza Kadoma, Kadoma-shi, Osaka
5718501 (JP).

(72) Inventors; and

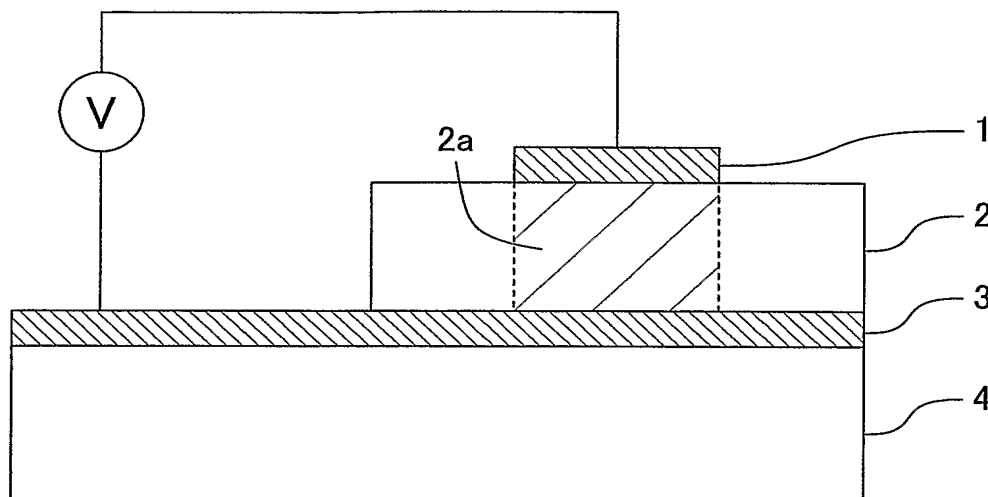
(75) Inventors/Applicants (for US only): **MURAOKA, Shun-
saku. OSANO, Koichi. TAKAHASHI, Ken. SHIMO-
TASHIRO, Masafumi.**

(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN,
CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI,
GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE,
KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD,
MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG,
PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM,
TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM,
ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI,
SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: MEMORY DEVICE, MEMORY CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT HAVING VARI-
ABLE RESISTANCE



(57) Abstract: A first variable resistor (5) is connected between a first terminal (7) and a third terminal (9) and increases/reduces its resistance value in accordance with the polarity of a pulse voltage applied between the first terminal (7) and the third terminal (9). A second variable resistor (6) is connected between the third terminal (9) and a second terminal (8) and increases/reduces its resistance value in accordance with the polarity of a pulse voltage applied between the third terminal (9) and the second terminal (8). Given pulse voltages are applied between the first terminal (7) and the third terminal (9) and between the third terminal (9) and the second terminal (8) to reversibly change the resistance values of the first and second variable resistors (5, 6), thereby recording one bit or multiple bits of information.

WO 2005/066969 A1



Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.